REMARKS

Claims 1-23 are pending.

Claims 1-23 are rejected.

The Applicants respectfully assert that the amendments to Claims 1-3, 4-7, 11-15, and 20-23 and incorporated by reference in any claims depending therefrom, are not narrowing amendments made for a reason related to the statutory requirements for a patent that will give rise to prosecution history estoppel. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831, 1839-40, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 234 F.3d 555, 566, 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2001).

EXAMINER INTERVIEW

The Applicant had a telephone interview with the Examiner to review the response to the Office Action. The Applicant explained that FIGS. 3A and 3B have been amended to label some of the nodes to clarify circuit partitions to make it easier to identify elements in the claims. The Applicant also discussed with the Examiner that the structure of the circuit of reference *Taguchi* was different from the circuitry in Claim 1. The Applicant pointed out that by identifying element 34 as the first cut-circuit of Claim 1, the Examiner has defined the domain output and domain input relative to Claim 1. The Examiner had stated that the domain input was not shown in reference *Taguchi*. The Examiner stated that he understood Applicant's argument and would review his response in light of Applicant's discussion. The Examiner thanked the Applicant for clarifying the drawings. The Applicant thanked the Examiner for discussing the claimed invention.

I. REJECTION UNDER 35 U.S.C. § 112

The Examiner rejected Claims 1, 3, 5, 20 and 22 under *35 U.S.C. § 112*, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claim 1 and Claim 20. In particular, the Examiner states that in Claim 1, line 4 it is not clear what applicant refers to as the domain output and the first output. The Examiner is directed to "replacement sheet" FIG. 4A where Applicant has added additional designators for clarification. The interface circuit of the present invention is between a first logic domain (C_Domain) and second logic domain (NC_Domain). C_ Domain has an output (domain output) that is coupled to the input of the interface circuit, thus "a first input (of the interface circuit) coupled to the domain output (output of C_Domain)." Likewise, the output of the interface circuit (first output) is coupled to the input of the NC_Domain (domain input). The input and output of the interface circuit comprise the multiple connections from sub-circuits at node 303 and 304, respectively, which the Applicant has tried to separate so that the inputs and outputs of the sub-circuits may be discussed relative to the claims.

Claims 1 and 20 has been amended to replace "first cut_inverter" with "first cut_circuit" to correct a typographical error which caused an antecedent basis problem.

Claim 3. Claim 2 has been amended to change "second" to "first" in line 3 and "the first logic state" to "a second logic state" and "first control" to "second control" in line 3 of Claim 2 to correct typographical errors. Claim 3 depends from Claim 2. Therefore, "first and second logic states" and "second control signal" have been introduced in Claim 2 and no longer represent an antecedent problem relative to Claim 3.

Claim 5. Claim 5 is dependent from Claim 1. Claim 5 has been amended to change "first cut_inverter" to "first cut_circuit" to correct a typographical error which in turn corrects the antecedent basis problem as "first cut_circuit" was introduced in Claim 1.

Claims 9, 10, and 20. The Examiner states that in Claim 9, 10, and 20 it is not clear what applicant refers to as the domain output and the first output. The Examiner is again directed to "replacement sheet" FIG. 4A where Applicant has added additional designators for clarification. The interface circuit of the present invention is between a first logic domain (C_Domain) and second logic domain (NC_Domain). C_ Domain has

an output (domain output) that is coupled to the input of the interface circuit, thus "a first input (of the interface circuit) coupled to the domain output (output of C_Domain)." Likewise, the output of the interface circuit (first output) is coupled to the input of the NC_Domain (domain input). The input and output of the interface circuit comprises the multiple connections from sub-circuits at node 303 and 304, respectively, which the Applicant has tried to separate so that the inputs and outputs of the sub-circuits may be discussed relative to the claims.

Claims 22. Claim 21 has been amended to change "second" to "first" in line 3 and "the first logic state" to "a second logic state" and "first control" to "second control" in line 3 of Claim 2 to correct typographical errors. Claim 3 depends from Claim 2. Therefore, "first and second logic states" and "second control signal" have been introduced in Claim 21 and no longer represent an antecedent problem relative to Claim 22.

II. REJECTION UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 1-19 under *35 U.S.C. § 103(a)* as being unpatentable over U.S. Patent No. 5,557,221 to *Taguchi et al.* (hereafter "*Taguchi*") in view U.S. Patent 6,862,226 to *Toyoda et al.* (hereafter "*Toyoda*").

Claim 1. The Examiner states that *Taguchi* teaches all the claimed features of FIG. 1. The Examiner states that element 1 of *Taguchi* is a first logic domain. Since element 1 only has one output line (32) shown it follows that the Examiner considers element 32 as the domain output (as recited in Claim 1). The Examiner then states that the domain input of a second logic domain is not shown. Therefore anything relative to the domain input and the second logic domain is not explicitly taught by *Taguchi*. Claim 1 specifically states that the interface circuit couples a domain output of a first logic circuit domain to a domain input of a second logic circuit domain.

The Examiner then states that element 34 of *Taguchi*, defined as transistors 36-39, is the first cut-circuit of Claim 1. The input of element 34 is coupled to the output of

NOR gate 33. Claim 1 recites that the input of the first cut-circuit is coupled to the domain output of a first logic domain. The input of element 34 of *Taguchi* is coupled to the output of a NOR gate that has two inputs; Pi and a control signal SGL. Therefore the input of element 34 is not coupled to the domain output of *Taguchi* as first stated by the Examiner, rather it is coupled to the output of element 33. Therefore, if element 35 is the first cut-circuit and element 32 is the domain output, then *Taguchi* does not teach or suggest an interface circuit with an input of a first cut-circuit coupled to a domain output as recited in Claim 1.

Claim 1 recites that the first cut-circuit has a first input coupled to the domain output and a first output coupled to the domain input. Since the Examiner states that element 34 of *Taguchi* is the first cut-circuit, then it follows that the first output of the first cut-circuit is the common drain connection of transistors 36-37. The first output of the first cut-circuit of Claim 1 is coupled to the domain input, thus for FIG. 1 to read on Claim 1 according to the Examiner, then the common drain connection of transistors 41-42 and the common gate connection of transistors 43-44 must be the domain input.

Since the Examiner states that element 32 is domain output (of Claim 1), then it follows that the Pi input of NOR gate 33 is the first input of the first cut-circuit. However the Examiner also states that element 34 is the first cut-circuit which implies that the common gate connection of transistors 36-37 is the first input of the first cut-circuit thus establishing a contradiction.

Likewise, if element 34 is the first cut-circuit, then the output of element 34 (drains of transistors 36 and 37) must be coupled to the domain input of the second logic domain. However, the Examiner states that the second logic domain is not shown. The Applicant asserts that the output of element 34 is clearly shown coupled to the drains of transistors 41 and 42 and the gates of transistors 43 and 44. Therefore, by the Examiners own argument, the node formed by the drains of transistors 41 and 42 and the gates of transistors 43 and 44 must be the domain input to the second logic domain. Therefore, by the Examiner's argument, the interface circuit that couples the output of the first logic

domain (output of NOR gate 33) to the second logic domain (drains of transistors 41 and 42 and the gates of transistors 43 and 44) is entirely element 34 of *Taguchi*.

Depending on which argument of the Examiner is used, either element 32 is the domain output or the output of NOR gate 33 is the domain output. Thus, by the same logic, either element 33 and element 34 constitute the first cut-circuit, or element 34 alone constitutes the first cut-circuit. In either case, the output of the first cut-circuit, using the Examiner's arguments, is the common drain connection of transistors 36 and 37.

Claim 1 states that the interface circuit coupling the domain output of the first logic domain to the domain input of a second logic domain comprises a first cut-circuit and a latch circuit. The Examiner states that the element 35 of *Taguchi* is a latch circuit wherein the latch circuit latches logic states at the domain input when the first voltage potential is decoupled form the first cut-circuit as recited by Claim 1. Element 35 consists of transistors 41-46 and inverter 47 and is a power-gated latch, however, it is not coupled to the first cut-circuit as recited in Claim 1. The input of element 35 (latch input) is the node consisting of the common drain connection of transistors 41 and 42 and the common gate connection of transistors 43 and 44. The output of element 35 (latch output) must therefore be the node formed by the common gate connection of transistors 41-42 and the common drain connection of transistors 43 and 44. To read on Claim 1, the latch input must be coupled to the first input of the first cut-circuit (domain output) and the latch output must be coupled to the first output of the first cut-circuit (domain input). If element 35 is the a latch circuit, then its input is only coupled to the output of element 34 and its output is only coupled to external inverter 48 not the domain output recited in Claim 1. By the above arguments it is obvious that *Taguchi* does not teach or suggest the circuit structure of Claim 1.

The Examiner states that *Taguchi* does not teach that the latch circuit having a latch input coupled to the first input (of the first cut-circuit), and a latch output coupled to the first output (of the first cut-circuit). By his own admission the Examiner states that *Taguchi* does not teach or suggest the circuit structure of Claim 1. Specifically, *Taguchi*

does not teach or suggest an interface circuit comprising a first cut-circuit having a first input coupled to a domain output, a first output coupled to a domain input and a latch circuit having a latch input coupled to the first input (of the first cut-circuit) and a latch output coupled to the first output (of the first cut-circuit). The latch circuit of Claim 1 is in parallel with the first cut-circuit. *Taguchi* does not teach or suggest any circuit in parallel with his element 34 (Examiner admitted first cut-circuit).

The Examiner states that *Toyoda* teaches a latch circuit comprising two inverters INV1 and INV2 which are coupled in parallel, the input of INV1 is coupled to the output of INV2 and the output of INV1 is coupled to the input of INV2. Therefore, by his own admission, the latch circuit of *Toyoda* is the parallel combination of INV1 and INV2. Therefore in FIG. 1 of *Toyoda*, the latch input is the common connection if IN1 and OUT2 and the latch output is the common connection of IN2 and OUT1. Again, the reference *Toyoda* does not teach or suggest a latch circuit in parallel with a first cut-circuit. The configuration of INV1 and INV2 of *Toyoda* operates as a latch to the extent that the signals on nodes 9 and 10, which set the state of the circuit formed by INV1 and INV2, can be removed (e.g., via pass transistors 5 and 6) and the circuit state will remain unchanged. Signals at inputs 9 and 10 must override the state of the circuit formed by INV1 and INV2 to change its state.

The teachings of *Toyoda* add nothing regarding the circuit structure of Claim 1, rather *Toyoda* teaches a circuit for driving a non-volatile flip-flop circuit using variable resistor elements. See Abstract and title of *Toyoda*. *Toyoda* does not teach or suggest and interface circuit between a first logic domain with a domain output and a second logic domain with a domain input. Claim 1 recites an interface circuit comprising a first cut-circuit and a latch (coupled in parallel) with a first input coupled to the domain input and a first output coupled to domain output. When the first cut-circuit is powered the signals from the first logic domain are coupled to the second power domain by action of the first cut-circuit. When the power supply is decoupled from the first cut-circuit the latch circuit then and only then latches logic states (coupled from the domain output) at the domain input through the parallel latch circuit.

In Claim 1 of the present invention, the inverter that is part of the latch circuit is in parallel to the first cut-circuit and has the same input and output signals as the first cut-circuit when the first cut-circuit is power-gated ON. When the first cut-circuit is power-gated OFF, the second cut-circuit of the latch circuit in Claim 1 is power-gated ON to provide the feedback so that the logic states on the domain input are held when the first cut-circuit is power-gated OFF.

Toyoda does not teach or suggest applying his latch circuit in parallel with any circuit. *Toyoda* only teaches a well known inverter configured flip-flop circuit which is driven by variable resistor elements. One of ordinary skill in the art would not arrive at the present invention in Claim 1 using the combination of *Toyoda* and *Taguchi* without hindsight of the present invention. The Applicant asserts that *Toyoda* adds nothing of substance to the teachings of *Taguchi* that would lead one of ordinary skill in the art to the present invention of Claim 1.

Therefore, the Applicant respectfully asserts that the rejection of Claim 1 under *35 U.S.C. § 103(a)* as being unpatentable over *Taguchi* in view of *Toyoda* is traversed by the above arguments.

Claims 2 and 19. Claim 2 has been amended to correct typographical errors. Amended Claim 2 is dependent from Claim 1 and contains all the limitations of Claim 1. The Applicant has shown that neither *Taguchi* or *Toyoda*, singly or in combination teach or suggest the invention of Claim 1. Claim 2 adds the limitation that the latch circuit is powered by the second voltage potential and a third voltage potential, and the third potential is coupled to the latch circuit in response to the first logic state of a second control signal and decoupled from the latch circuit in response to the second logic state of the second control signal. *Toyoda* does not teach or suggest a latch circuit that is power-gated. The Applicant has shown that *Toyoda* does not teach or suggest coupling any latch circuit (power-gated or not) in parallel with a first cut-circuit. The Examiner by his own admission admits that *Taguchi* does not teach the circuit structure of Claim 1 where the first cut-circuit is coupled in parallel with the latch circuit. The Examiner states that the latch circuit (element 35) is powered by the second voltage potential and a third voltage

(another Vcc). The Examiner has stated that *Taguchi* only shows a first logic domain. *Taguchi* only shows one VCC, therefore *Taguchi* does not teach or suggest a third voltage potential. The Examiner states that element 35 is a latch with a third voltage potential coupled in response to the logic 1 state of the first control signal (CONT SGL). The only voltage potential that is coupled to the Examiner's latch (element 35) is VCC which is the first voltage potential (by the Examiner's own admission relative to Claim 1).

The Applicant has shown that *Taguchi* does not teach or suggest the circuit of Claim 1, therefore cannot teach the invention of Claim 2 which further limits Claim 1. The Examiner does not state that *Toyoda* teaches or suggests the invention of Claim 2. Therefore, the Applicant respectfully asserts that the rejection of Claim 2 under *35 U.S.C. § 103(a)* as being unpatentable over *Taguchi* in view of *Toyoda* is traversed by the above arguments and for the same reasons as Claim 1.

Claim 19 is dependent from Claim 2 and contains all the limitations of Claim 2. Claim 19 adds the limitation that the first and third voltage potentials are equal. The Examiner rejected Claim 19 for the same reason as Claim 2. The Applicant has shown that neither *Taguchi* or *Toyoda*, singly or in combination, teach or suggest the invention of Claim 1 and thus do not teach the limitation of Claim 2. Therefore, the Applicant respectfully asserts that the rejection of Claim 2 under *35 U.S.C. § 103(a)* as being unpatentable over *Taguchi* in view of *Toyoda* is traversed by the above arguments and for the same reasons as Claim 1.

Claims 3 and 4. Claim 3 is dependent from Claim 2 and contains all the limitations of Claim 2. Claim 3 adds the limitations to Claim 2. The Applicant has shown that neither *Taguchi* or *Toyoda*, singly or in combination, teach or suggest the invention of Claim 2 and thus do not teach the limitation of Claim 3. Therefore, the Applicant respectfully asserts that the rejection of Claim 3 under *35 U.S.C. § 103(a)* as being unpatentable over *Taguchi* in view of *Toyoda* is traversed by the above arguments and for the same reasons as Claim 1.

Claim 4 is dependent from Claim 3 and contains all the limitations of Claim 3. Claim 4 adds the limitations to Claim 3. The Examiner rejected Claim 4 for the same reasons as Claim 3. The Applicant has shown that neither *Taguchi* or *Toyoda*, singly or in combination, teach or suggest the invention of Claim 2 and thus do not teach the invention of Claim 4. Therefore, the Applicant respectfully asserts that the rejection of Claim 4 under *35 U.S.C. § 103(a)* as being unpatentable over *Taguchi* in view of *Toyoda* is traversed by the above arguments and for the same reasons as Claim 1.

Claim 5. Claim 5 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 1 adds the limitations to Claim 1. The Applicant has shown that neither *Taguchi* or *Toyoda*, singly or in combination, teach or suggest the invention of Claim 1 and thus do not teach the invention of Claim 5. Therefore, the Applicant respectfully asserts that the rejection of Claim 4 under *35 U.S.C. § 103(a)* as being unpatentable over *Taguchi* in view of *Toyoda* is traversed by the above arguments and for the same reasons as Claim 1.

Claims 6-18. The Examiner rejected Claims 6-18 for the same reasons as Claims 1-5. Claims 6-18 add additional limitations to Claims 1 and 5. Since the Examiner has failed to specifically address these claims, the Applicant asserts that the Examiner has failed to make a prima facie case of obviousness over *Taguchi* in view of *Toyoda*. Further The Applicant has shown that neither *Taguchi* or *Toyoda*, singly or in combination, teach or suggest the invention of Claim 1 and thus do not teach the inventions in Claims 6-18. Therefore, the Applicant respectfully asserts that the rejection of Claim 4 under *35 U.S.C. § 103(a)* as being unpatentable over *Taguchi* in view of *Toyoda* is traversed by the above arguments and for the same reasons as Claims 1-5.

The Examiner rejected Claims 20-24 under *35 U.S.C. § 103(a)* as being unpatentable over U.S. Patent No. 6,275,077 to *Tobin et al.* (hereafter "*Tobin*") in view *Taguchi* and further in view of *Toyoda*.

Claim 20. The Examiner relies on *Tobin* to teach all the features of the data processing system of Claim 20 and *Taguchi* to teach all of the elements and their

relationships regarding the details of the interface circuit. The interface circuit of Claim 20 is the same as the interface circuit of Claim 1. The Applicant has shown that *Taguchi* does not teach or suggest the invention of Claim 1. By his own admission, the Examiner states that *Taguchi* does not teach or suggest the configuration of the latch and the first cut-circuit of Claim 1. The Examiner relies no *Toyoda* to teach the configuration of the latch and first cut-circuit of Claim 1. The Applicant has shown that neither *Toyoda* and *Taguchi*, singly or in combination teach or suggest all of the limitations of Claim 1, therefore they do not teach or suggest the data processing system of Claim 20 which includes the interface circuit of Claim 1.

Therefore, the Applicant respectfully asserts that the rejection of Claim 20 under *35 U.S.C. § 103(a)* as being unpatentable over *Tobin* in view of *Taguchi* and further in view of *Toyoda* is traversed by the above arguments and for the same reasons as Claim 1.

Claims 21 and 24. Claims 21 and 24 are dependent from Claim 20. Claim 21 adds the same limitation to Claim 20 as Claim 2 adds to Claim 1. Likewise, Claim 24 adds the same limitation to Claim 20 as Claim 5 adds to Claim 1. The Examiner relies on *Tobin* to teach all the features of the data processing system of Claim 20 and *Taguchi* to teach all of the elements and their relationships regarding the details of the interface circuit. The interface circuit of Claim 20 is the same as the interface circuit of Claim 1. The Applicant has shown that *Taguchi* does not teach or suggest the inventions of Claims 2 and 5.

Therefore, the Applicant respectfully asserts that the rejections of Claims 21 and 24 under *35 U.S.C. § 103(a)* as being unpatentable over *Tobin* in view of *Taguchi* and further in view of *Toyoda* is traversed by the above arguments and for the same reasons as Claims 1, 2 and 5.

Claims 22 and 23. Claims 22 is dependent from Claim 21 and Claim 23 is dependent from Claim 22. Claim 22 adds the same limitation to Claim 21 as Claim 3 adds to Claim 2. Likewise, Claim 23 adds the same limitation to Claim 22 as Claim 4 adds to Claim 3. The Examiner relies on *Tobin* to teach all the features of the data

processing system of Claim 20 and *Taguchi* to teach all of the elements and their relationships regarding the details of the interface circuit. The interface circuit of Claim 20 is the same as the interface circuit of Claim 1. The Applicant has shown that *Taguchi* does not teach or suggest the inventions of Claims 3 and 4.

Therefore, the Applicant respectfully asserts that the rejections of Claims 22 and 23 under *35 U.S.C. § 103(a)* as being unpatentable over *Tobin* in view of *Taguchi* and further in view of *Toyoda* is traversed by the above arguments and for the same reasons as Claims 1, 2, 3, and 4.

II. CONCLUSION

The Applicant has traversed the rejections of Claims 1-19 under *35 U.S.C. § 103(a)* as being unpatentable over *Taguchi* in view of *Toyoda.*

The Applicant has traversed the rejections of Claims 20-24 under *35 U.S.C. § 103(a)* as being unpatentable over *Taguchi* in view of *Toyoda* and further in view of *Tobin.*

The Applicant has amended Claims 1-3, 4-7, 11-15, and 20-23 to correct informalities because of typographical errors.

The Applicant asserts that Claims 1-24 as amended are now in condition for allowance and request early allowance of these claims

Applicants respectfully request that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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IN THE DRAWINGS

Replacement drawings for FIGS. 3A and 4A have been included. Designators have been added to key inputs and outputs to make the claims more clear. Particularly a designator "V3" has been added to identify the "third voltage potential." Some of the nodes have been separated so that it is clearer what is the latch input, latch output, first input, second input, domain input, domain output, power nodes N1 and N2 for the first cut circuit, and power nodes LN1 and LN2 for the latch circuit.